Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 52945

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to B.E. Electronics and Instrumentation Engineering/B.E. Instrumentation and Control Engineering)

(Regulation 2013)

(Also common to: PTEE 6301 – Digital Logic circuits for B.E. (Part-Time) Third Semester – Electrical and Electronics Engineering Regulation 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert a binary number $(1101101)_2$ to decimal and octal numbers.

2. Define Tri-state gates.

3. Write the logic expression for Full adder and Full subtractor.

4. What is meant by canonical form? Give an example for POS and SOP canonical forms.

5. Draw the sequential logic diagram for Parallel In — Serial Out Shift register.

6. Write the characteristic equation of JK flip flop and its truth table.

7. Define race condition. How it can be eliminated.

8. Describe PROM.

9. List the purpose of Test bench.

10. Design a Half adder using HDL

PART B — (5 × 13 = 65 marks)

11. (a) Define Binary code. Demonstrate the Hamming code with an example. (13)

Or

(b) Explain TTL logic in detail along with its types. (13)

12. (a) Design a Combinational logic circuit to convert Binary to Gray code and write its truth table. (13)

Or

(b) Implement the following Boolean function using 4:1 Multiplexer. (13)

$F(W, X, Y, Z) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$

13. (a) Synthesis a 3 bit counter using T Flip Flop (State diagram, Excitation table, K-map, Logic diagram). (13)

Or

(b) What is meant by a Flip Flop? Write the characteristics equation, characteristics table and draw logic of SR, JK and D flip flops. (2+4+4+3)

14. (a) Explain the steps for the design of Asynchronous sequential circuits with an example. (13)

Or

(b) Draw a PLA circuit to implement the functions (13)

$F_1 = AB' + AC + A' BC'$ and $F_2 = (AC + BC)'$.

15. (a) Describe RTL in HDL with an example.

Or

(b) (i) Write the HDL program for 2:1 multiplexer in Dataflow and Behavioral Description. (6)

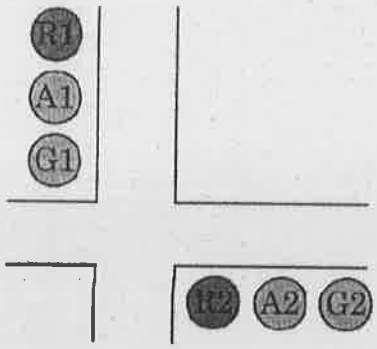
(ii) Write program in HDL to design 2 bit up/down counter. (7)

PART C — (1 × 15 = 15 marks)

16. (a) Design an asynchronous circuit that has two inputs X_1 and X_2 and one output Z. The circuit is required to give an output whenever the input sequence (0, 0) (0, 1) and (1, 1) received but only in that order. Design it using T flip flop. (15)

Or

(b) Design a synchronous digital circuit, a Moore machine, which operates this traffic light at two types of road crossing.



Quiet Junction

Red	Green
Red	Amber
Green	Red
Amber	Red

Busy Junction

Red	Green
Red	Amber
Red	Red
Green	Red
Amber	Red
Red	Red